

PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete If Known	
				Application / Conf. No.	Unknown /
				Filing Date	February 20, 2004
				First Named Inventor	Tim Tuan
				Art Unit	Unknown
				Examiner Name	Unknown
				Attorney Docket Number	X-1462-1P US
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature	<i>Nelson Lam</i>	Date Considered	3/9/06
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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[illegible]

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Complete if Known

Application / Conf. No.	10/783,216 /
Filing Date	February 20, 2004
First Named Inventor	Tim Tuan
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-1462-1P US

(use as many sheets as necessary)

Sheet	1	of	2
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Sheet	2	of	2	Attorney Docket Number	X-1462-1P US

OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
NL		MUTOH, S. et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," August 1995, pages 847-854, Vol. 30, No. 8, available from IEEE Journal of Solid-State Circuits, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
NL		KURODA, T., et al., "A 0.9V, 150-MHz, 1-mW, 4 mm ² 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage (VT) Scheme, 1996, pages 1770-1779, Vol. 31, No. 11, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
NL		INUKAI, T. et al., "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," 2000, pages 409-412, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
NL		HAMZAOGLU, F. et al., "Circuit-Level Techniques to Control Gate Leakage for sub-100nm CMOS," ISLPED, August 12-14, 2002, Pages 60-63, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	

Examiner Signature	<i>Nelson Lee</i>	Date Considered	3/9/06
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of

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Complete if Known

Application / Conf. No.	10/783,216	/	6678
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Filing Date	February 20, 2004
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First Named Inventor	Tim Tuan
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Art Unit	2816
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Examiner Name	Unknown
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Attorney Docket Number	X-1462-1P US
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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**Examiner
Signature**

Nelson L

Date Considered

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NL		Jae Y. Park, Mark G. Allen; "A Comparison of Micromachined Inductors with Different Magnetic Core Materials"; 1996 Electronic Components and Technology Conference; 1996 IEEE; pp. 375-381.	
NL		Thomas D. Burd et al.; "A Dynamic Voltage Scaled Microprocessor System"; 2000 IEEE; IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000; pp. 1571-1580.	
NL		Anthony J. Stratakis et al.; "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System"; 1994 IEEE; pp. 619-626.	
NL		Anthony John Stratakis; "High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications," Chapter 3; "DC-DC Converter Fundamentals"; pp. 42-78.	

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